34. (original) The method of claim 32, wherein enabling erasure further comprises enabling erasure by coupling a chip test probe to a bond pad of a lock bit erase circuit when the Flash memory is in wafer form.

35. (original) The method of claim 32, wherein disabling erasure further comprises disabling erasure by not coupling a bond pad of a lock bit erase circuit to an external connector of the Flash memory device in packaged form.

36. (Currently Amended) A method of erase enabling the lock bits of a protection register comprising:

forming a floating gate erase circuit coupled to one or more lock bits of a protection register; and

forming a lock bit erase enable circuit coupled to the floating gate erase circuit, wherein the ~~erase block~~ lock bit erase enable circuit is operable only when an integrated circuit containing the protection register is in wafer form.

37. (Currently Amended) The method of claim 36, wherein forming the ~~erase block~~ lock bit erase enable circuit further comprises:

forming a bond pad;

forming an input buffer, wherein an input of the input buffer is coupled to the bond pad and where an output of the input buffer is coupled to ~~a~~ the floating gate erase circuit.

38. (original) The method of claim 37, wherein forming the lock bit erase enable circuit further comprises:

forming a first pull down transistor, wherein the first pull down transistor is a weak pull down transistor;

forming a second pull down transistor, wherein the first and second pull down transistors are each coupled to the input of the input buffer and to ground;

forming an inverter coupled to an output of the input buffer and to a gate of the first pull